

Titanium FPGA Selector Guide

35K to 1,000K Logic Elements	10 Kb Embedded RAM Blocks	DSP Blocks	PLLs	High-Voltage I/O (HVIO)	High-Speed I/O (HSIO)	MIPI D-PHY 2.5 Gbps	LPDDR4/4x Controller & PHY	SerDes 16G/25.8G

Titanium Ordering Codes

You can use HSIO pairs for a various differential standards such as LVDS (1.5 Gbps), differential HSTL/SSTL, or MIPI RX and TX data/clock lanes (1.5 Gbps).

FPGA	LEs	RAM (Mbits)	RAM Blocks (10 Kb)	DSP Blocks	Package	Pins	HVIO	HSIO	PLLs	2.5G MIPI D-PHY	LPDDR4/4x 2.6 Gbps	LPDDR4/4x 3.733 Gbps	16G SerDes	PCIe Gen4	25.8G SerDes	Temperature	Speed Grade	Ordering Code				
Ti35	36,176	1.53	149	93	FBGA	100	-	61	3	-	-	-	-	-	-	C	3, 3L, 4, 4L	Ti35F100S3F2C3/3L/4/4L				
																I	3, 3L	Ti35F100S3F2I3/3L				
					FBGA	225	23	140	4	-	-	-	-	-	-	-	-	-	C	3, 3L, 4, 4L	Ti35F225C3/3L/4/4L	
																			I	3, 3L	Ti35F225I3/3L	
Ti60	62,016	2.6	256	160	WLCSP	64	-	35	2	-	-	-	-	-	-	-	C	3	Ti60W64C3			
					FBGA	100 (1)	-	61	3	-	-	-	-	-	-	-	-	-	C	3, 3L, 4, 4L	Ti60F100S3F2C3/3L/4/4L	
																			I	3, 3L	Ti60F100S3F2I3/3L	
					FBGA	225	23	140	4	-	-	-	-	-	-	-	-	-	-	C	3, 3L, 4, 4L	Ti60F225C3/3L/4/4L
																				I	3, 3L	Ti60F225I3/3L
					Ti90	92,534	6.88	671	336	FBGA	361	20	110	8	2TX 2RX	x16	-	-	-	-	-	C
I	3, 3L, 4, 4L	Ti90M361I3/3L/4/4L																				
2TX 2RX	-	x16	-	-											-	-	C	3, 3L, 4, 4L	Ti90J361C3/3L/4/4L			
I	3, 3L, 4, 4L	Ti90J361I3/3L/4/4L																				
4 TX 4 RX	-	-	-	-											-	C	3, 3L, 4, 4L	Ti90L484C3/3L/4/4L				
I	3, 3L, 4, 4L	Ti90L484I3/3L/4/4L																				
484	27	116	8	4 TX 4 RX							x16	-	-	-	-	C	3, 3L, 4, 4L	Ti90M484C3/3L/4/4L				
				I							3, 3L, 4, 4L	Ti90M484I3/3L/4/4L										
				4 TX 4 RX							-	x16 x32	-	-	-	C	3, 3L, 4, 4L	Ti90J484C3/3L/4/4L				
				I							3, 3L, 4, 4L	Ti90J484I3/3L/4/4L										
				-							x16	-	-	-	-	C	3, 3L, 4, 4L	Ti90F529C3/3L/4/4L				
				I							3, 3L, 4, 4L	Ti90F529I3/3L/4/4L										
529	48	210	8	-	-	x16 x32	-	-	-	C	3, 3L, 4, 4L	Ti90G529C3/3L/4/4L										
				I	3, 3L, 4, 4L	Ti90G529I3/3L/4/4L																

1. The Ti60 FPGA in the F100 pin package is a SIP that incorporates SPI flash and HyperRAM in addition to the Ti60 FPGA.

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FPGA	LEs	RAM (Mbits)	RAM Blocks (10 Kb)	DSP Blocks	Package	Pins	HVIO	HSIO	PLLs	2.5G MIPI D-PHY	LPDDR4/4x 2.6 Gbps	LPDDR4/4x 3.733 Gbps	16G SerDes	PCIe Gen4	25.8G SerDes	Temperature	Speed Grade	Ordering Code	
Ti120	123,379	9.18	896	448	FBGA	361	20	110	8	2TX 2RX	x16	-	-	-	-	-	C	3, 3L, 4, 4L	Ti120M361C3/3L/4/4L
										I	Ti120M361I3/3L/4/4L								
										2TX 2RX	-	x16	-	-	-	-	C	3, 3L, 4, 4L	Ti120J361C3/3L/4/4L
										I	Ti120J361I3/3L/4/4L								
						484	27	116	8	4 TX 4 RX	-	-	-	-	C	3, 3L, 4, 4L	Ti120L484C3/3L/4/4L		
										I	Ti120L484I3/3L/4/4L								
										4 TX 4 RX	x16	-	-	-	-	C	3, 3L, 4, 4L	Ti120M484C3/3L/4/4L	
										I	Ti120M484I3/3L/4/4L								
						4 TX 4 RX	-	x16 x32	-	-	-	-	C	3, 3L, 4, 4L	Ti120J484C3/3L/4/4L				
						I	Ti120J484I3/3L/4/4L												
						529	48	210	8	-	x16	-	-	-	-	C	3, 3L, 4, 4L	Ti120F529C3/3L/4/4L	
										I	Ti120F529I3/3L/4/4L								
-	-	x16 x32	-	-	-					-	C	3, 3L, 4, 4L	Ti120G529C3/3L/4/4L						
I	Ti120G529I3/3L/4/4L																		
Ti180	176,256	13.11	1,280	640	FBGA	361	20	110	8	2TX 2RX	x16	-	-	-	-	-	C	3, 3L, 4, 4L	Ti180M361C3/3L/4/4L
										I	Ti180M361I3/3L/4/4L								
										2TX 2RX	-	x16	-	-	-	-	C	3, 3L, 4, 4L	Ti180J361C3/3L/4/4L
										I	Ti180J361I3/3L/4/4L								
						484	27	116	8	4 TX 4 RX	-	-	-	-	C	3, 3L, 4, 4L	Ti180L484C3/3L/4/4L		
										I	Ti180L484I3/3L/4/4L								
										4 TX 4 RX	x16	-	-	-	-	-	C	3, 3L, 4, 4L	Ti180M484C3/3L/4/4L
										I	Ti180M484I3/3L/4/4L								
						4 TX 4 RX	-	x16 x32	-	-	-	-	C	3, 3L, 4, 4L	Ti180J484C3/3L/4/4L				
						I	Ti180J484I3/3L/4/4L												
						529	48	210	8	-	x16	-	-	-	-	C	3, 3L, 4, 4L	Ti180F529C3/3L/4/4L	
										I	Ti180F529I3/3L/4/4L								
-	-	x16 x32	-	-	-					-	C	3, 3L, 4, 4L	Ti180G529C3/3L/4/4L						
I	Ti180G529I3/3L/4/4L																		

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Package Dimensions

Package	Pitch	Dimensions (mm)
64-ball FBGA	0.4	3.5x3.4
100-ball FBGA	0.5	5.5x5.5

Package	Pitch	Dimensions (mm)
225-ball FBGA	0.65	10x10
361-ball FBGA	0.65	13x13

Package	Pitch	Dimensions (mm)
484-ball FBGA	0.8	18x18
529-ball FBGA	0.8	19x19

Example Ordering Code

Titanium FPGA — **Ti60 F 225 C 3**

Package Code

F: FBGA, without hard MIPI, DDR at 2.6 Gbps
G: FBGA, without hard MIPI, DDR at 3.733 Gbps
J: FBGA, with hard MIPI, DDR at 3.733 Gbps
L: FBGA, with hard MIPI
M: FBGA, with hard MIPI, DDR at 2.6 Gbps
S3F2: FBGA, with HyperRAM and Flash
W: Wafer-Level Chip-Scale Package

Speed Grade

3, 3L, 4, 4L (L is low power)
Higher numbers are faster

Operating Temperature

C: Commercial ($T_j = 0^\circ\text{C}$ to 85°C)
I: Industrial ($T_j = -40^\circ\text{C}$ to 100°C)

Number of Pins

Some ordering codes include extra characters after the pin count to designate additional components in the package. For example, the Ti60 in the F100 package has HyperRAM and flash as indicated by the S3F2 after the number of pins.